Design and Implementation of a Wireless Transmission Signal Simulation System Based on STM32

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Abstract. This paper designs and implements a wireless transmission signal simulation system, addressing the characteristics of line-of-sight and multipath signal propagation in wireless communication systems. The system is centered around the STM32F103RCT6 microcontroller, which controls the AD9959 quad-channel Direct Digital Synthesizer (DDS) via the SPI interface to generate multi-channel radio frequency baseband signals. For precise amplitude adjustment, an AD8367 variable gain amplifier is employed, utilizing its precise logarithmic voltage control gain function. Signal mixing and multipath synthesis are achieved using an AD835 four-quadrant analog multiplier. After filtering to remove sampling distortion, the line-of-sight signal and delayed multipath components are additively synthesized to produce the simulated wireless transmission signal. Experimental results demonstrate the system's ability to stably generate multi-channel signals with adjustable amplitude and phase, meeting design specifications. Specifically, the output error for modulation depth ranges from 30% to 90% is within 3%. For amplitude attenuation from 0 to 12dB, the attenuation error is within 0.2dB. Furthermore, for delays between 50 ns and 200 ns and phases between 0° and 150°, the actual output error compared to set values is minimal and within an acceptable range (not exceeding 5%). This makes the system an effective tool for wireless channel simulation and communication testing.

Keywords: Wireless signal simulation; Multipath fading; Direct Digital Synthesis (DDS); AD8367; AD835; STM32

1. Introduction

In modern wireless communication systems, signals are inevitably subjected to complex environmental influences during propagation, such as building reflections, ground diffraction, and vegetation scattering. These factors often cause signals to arrive at the receiving end

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through multiple paths, forming what is known as "multipath signals"[1]. The multipath effect is a core issue in wireless communication, causing a series of problems such as delay spread, frequency-selective fading, phase distortion, and inter-symbol interference in the received signal, severely degrading communication quality and system performance. For instance, in wireless mobile communication multipath environments, signals transmitted by mobile terminals may not reach the base station directly due to obstacles; instead, they undergo diffraction and scattering, creating an angle spread effect and generating clustered local diffusion multipath signal sources. This complex channel characteristic makes it difficult for traditional point source models to accurately describe signal propagation. Therefore, constructing a signal simulation system capable of replicating actual channel effects is crucial for the research and development of communication equipment, performance testing, and related algorithm verification.

Currently, there are some mature channel simulation devices available internationally, such as products from companies like Keysight and Spirent. These devices are powerful and offer excellent performance. However, they are typically expensive, which hinders their widespread use in common teaching and research environments. To address this deficiency, this study is dedicated to designing and implementing a low-cost, easy-to-operate multi-channel wireless transmission signal simulation system. By precisely controlling parameters such as signal frequency, amplitude, phase, and delay, the system aims to simulate wireless line-of-sight and multipath transmission environments, providing an economical and efficient alternative for communication equipment testing and algorithm verification.

In recent years, the design of wireless communication systems based on microcontrollers (such as STM32) has become a popular research direction. Direct Digital Synthesis (DDS) technology, due to its advantages of high resolution, fast switching, wide frequency range, and precise phase control, has been widely applied in the field of signal generation[2]. For example, the AD9959, a four-channel DDS chip, can provide multiple independently controllable RF outputs, making it very suitable for generating the multiple components required for multipath signals. All channels of the AD9959 share a system clock and have natural synchronization, making it suitable for generating multiple coherent signals. Its high-speed 16-bit DAC can perform high-order modulation and is widely used in test and measurement, radar, communication, and other fields. Meanwhile, the STM32F103 series microcontroller, based on the 72 MHz ARM Cortex-M3 core, possesses rich peripheral interfaces and high-speed computing capabilities, enabling real-time control and multi-channel data processing. By combining DDS technology with

variable gain amplifiers and analog multipliers, baseband signals can be generated in the digital domain with precise amplitude control and mixing processing, thereby effectively simulating real multipath transmission channels.

This paper will provide a detailed introduction to the hardware composition, software implementation, and key technologies of the designed wireless transmission signal simulation system, including DDS signal generation, signal amplitude adjustment, multipath signal mixing and synthesis, and filtering. Through the research and implementation of this system, we hope to provide a practical, flexible, and cost-effective solution for the field of wireless channel simulation.

2. Methodology

2.1. System Overall Block Diagram

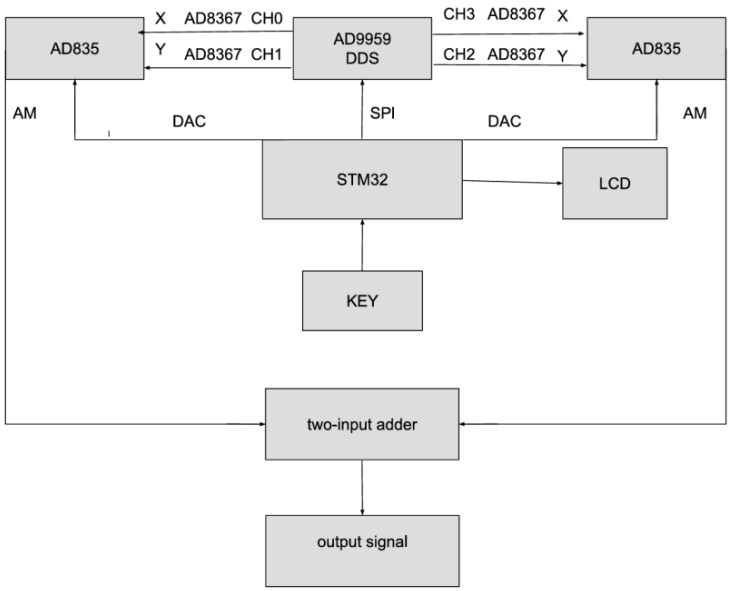

Figure 1. Overall System Block Diagram.

The overall system block diagram is shown in Figure 1. The STM32F103 configures the parameters (frequency, phase, amplitude) of each channel of the AD9959 via the SPI bus to generate digital signal sources[3]. The four DDS output signals are input to the AD8367 variable gain amplifier for flexible amplitude control.A portion of the amplified signal is directly output as a "direct path" signal, and the other portion is mixed with the delayed baseband signal generated by the STM32 via DAC through the AD835 analog multiplier, to generate the "multipath" component,which is finally superimposed and output through a passive combiner. The entire system also includes a power regulation module and a button/display

interface for system power-on, parameter setting, and monitoring. This design utilizes the AD9959's built-in four synchronized DDS cores, which can generate multiple mutually coherent sine waves or modulated signals. The STM32F103 provides high-speed computing and various communication interfaces to meet the requirements for signal generation and control.

2.2. Scheme Comparison and Selection

2.2.1. Signal Waveform Generation Scheme Selection

Scheme 1: LM6321 is a precision oscillator produced by National Semiconductor (now acquired by Analog Devices). It is primarily used in industrial applications, especially where stable, low-noise signals are required. The LM6321 is known for its excellent frequency stability and temperature drift control, making it very suitable for long-life, continuously operating circuits. Its internal design helps reduce noise, which is very important for equipment requiring a high signal-to-noise ratio, such as audio signal chains.

Scheme 2: AD9850 is a high-performance digital-to-analog converter (DAC) produced by Analog Devices. It is often used in applications such as audio signal processing, image display, and industrial control systems. As a 12-bit or 14-bit DAC, the AD9850 provides extremely high conversion accuracy, suitable for applications with very high demands on signal quality. It supports sampling rates up to 40 MSPS (Million Samples Per Second), enabling real-time data transmission.

Scheme 3: AD9959 is a high-performance Direct Digital Synthesizer (DDS). The features of AD9959 include high precision, high speed, multi-channel capability, and flexible interface. The AD9959 has four independent, programmable DDS channels, each capable of independently generating sine waveforms of different frequencies, phases, and amplitudes. All channels share a system clock, ensuring phase synchronization of multiple output signals, which is crucial for simulating coherent multipath signals[2]. It also has built-in noise reduction circuits, sample-and-hold, and data calibration to improve conversion quality and stability.

Although Scheme 1, the LM6321, is an industrial-grade product, it may not be as miniaturized as modern, more compact on-chip oscillators, and its power consumption may be relatively higher. Also, newer products may have more advanced performance, and the LM6321 may no longer be the latest technology choice. Therefore, Scheme 1 is excluded. Scheme 2, the AD9850, may consume more power in high-speed operating mode, which might not be ideal for battery-powered or energy-limited applications. Therefore, Scheme 2 is excluded. Scheme 3, the AD9959's four-channel synchronous output characteristic can effectively reduce phase

deviation between multiple signals, ensuring the coherence of the system's signals. In audio applications, the AD9959's high sampling rate can ensure the details and integrity of sound quality and reduce distortion when capturing and analyzing audio signals. Although it is a high-performance device, in audio applications, by selecting appropriate power management and operating modes, the AD9959 can still maintain relatively low power consumption.

In summary, the AD9959 is very suitable for professional audio equipment with high demands on audio quality, such as audio interface cards, digital audio processors, etc. Therefore, Scheme 3 is selected.

2.2.2. CPU Processing Module Scheme Selection

Scheme 1: AT89C51 is a classic 8-bit microcontroller belonging to the MCS-51 series, produced by Philips. Due to its mature technology and wide compatibility, it is widely used in industrial control, embedded systems, consumer electronics, and other fields. As an early MCU, its cost is relatively low, making it very economical for entry-level learners and small project development.

Scheme 2: STM32F103RCT6 is a microcontroller based on the ARM Cortex-M3 core, widely used on ST's CubeMX development platform. It adopts a 32-bit processor with fast processing speed and high real-time task processing capability. It has rich built-in peripherals such as ADC, DAC, USART, I2C, SPI and other communication interfaces, as well as timers, PWM, GPIO, etc., which can meet various application requirements. It has multiple general-purpose I/O pins, which are convenient for connecting external sensors and actuators, and has good scalability. The STM32F103 series microcontroller demonstrates strong scalability and real-time performance in wireless signal simulation system design with its rich peripheral interfaces and high-speed computing capabilities[4].

Compared with modern microcontrollers, Scheme 1, the AT89C51, has a slower processing speed and low data throughput. The storage space is small, with only a mere 128B of RAM, which may be insufficient for complex projects. Therefore, Scheme 1 is excluded. Scheme 2 includes Flash memory (up to 128KB to 512KB) and SRAM (up to 192KB), which meet the needs for program storage and data processing. At the same time, it integrates online debugging functions and supports third-party IDEs such as Keil MDK, resulting in high development efficiency.

In summary, Scheme 2 is selected.

2.2.3. Modulation Module Scheme Selection

Scheme 1: MAX4208 is an integrated isolated data acquisition and converter. It has a complete built-in signal chain, including voltage isolation, analog front-end, ADC, and digital I/O, simplifying system design. It typically provides electrical safety protection up to several thousand volts. Its high-speed data transmission is suitable for real-time or high-speed applications. It comes with a self-calibration function, reducing the need for external components.

Scheme 2: AD840 is a very classic linear operational amplifier produced by Texas Instruments (TI). It is known for its high input impedance, low offset voltage, high common-mode rejection ratio, and wide bandwidth characteristics. It boasts extremely high common-mode rejection ratio and ultra-low offset voltage performance. It is suitable for applications ranging from audio to microwave and can be used as a general-purpose gain device.

Scheme 3: AD835 is particularly suitable for signal processing applications requiring high-precision linear conversion due to its high input impedance, low offset, and excellent common-mode rejection[5]. Because of its stability, the AD835 can perform the multiplication of two analog signals with high precision. It is often used to implement precise voltage references or threshold detection; as a feedback component, it can build high-pass, low-pass, or band-pass filters, especially in audio and communication systems.

Scheme 1, the MAX4208, integrates a large number of functions, which may lead to a higher cost compared to purchasing components separately. Although it offers various configuration options, the degree of customization may be less flexible than with discrete components. In this design, it may require specialized power management circuits, increasing additional power consumption and complexity, so Scheme 1 is excluded. Scheme 2, the AD840, may consume significant power in high-performance operation, which might lead to lower efficiency, thus Scheme 2 is excluded. Scheme 3, the AD835, can stably measure phase difference through its high gain characteristic in this design. Meanwhile, the AD835 has extremely high common-mode rejection ratio (CMRR) and input bias current (IBI), which allows it to provide excellent DC and AC performance in signal processing applications.

In summary, Scheme 3 is selected.

2.2.4. Amplifier Circuit Scheme Selection

Scheme 1: Operational Amplifier (Op-Amp), due to its unique performance characteristics, is widely used in electronic engineering. Op-amps can provide an extremely high input-output ratio, theoretically infinite, which allows them to amplify weak signals. The input terminal has

almost no effect on the signal source, reducing the impact of the signal source load and protecting the signal source from damage.

Scheme 2: Field-Effect Transistor (FET) amplifier is an amplifier circuit designed using FETs as the basic switching element. Since the FET's gate has almost no current influence on the source, the input resistance is very high, making it suitable for small signal transmission between the signal source and the amplifier. Typically using common-drain or common-gate topology, it can provide better DC and AC characteristics and low noise.

Scheme 3: AD8367 is a high-voltage voltage-controlled gain amplifier designed by Analog Devices, mainly used for linear amplification and frequency response control in audio and communication systems. The AD8367 is a true RMS responding variable gain amplifier with precise logarithmic voltage control gain function, offering a wide gain range and high linearity[6]. It can provide a wide gain range, allowing the signal to be effectively amplified in various application scenarios. Due to its high-performance internal architecture, the AD8367 can maintain good performance under both large and small signal conditions, adapting to rapidly changing signal environments.

Although Scheme 1 has very high input impedance, the introduced noise needs to be considered in some applications. At the same time, some low-power models of op-amps are only suitable for small current or micropower applications, so Scheme 1 is excluded. In Scheme 2, if the gate control is improper, there may be larger leakage current, which will increase power consumption and may affect accuracy. Also, some FET models may not be as easily available or as affordable as ordinary transistors, so Scheme 2 is excluded. Scheme 3's voltage-controlled gain allows it to automatically adjust the gain according to the change in input voltage, which is very useful in situations requiring precise dynamic range control and sound shaping. At the same time, the carefully designed circuit structure helps reduce nonlinear distortion and ensures high-quality output signals.

In summary, Scheme 3 is selected.

2.2.5. Power Supply Scheme Selection

Scheme 1: LT3045 is a linear regulator. It is an integrated high-performance, low-ripple current mode switching regulator, suitable for applications requiring high efficiency and small packaging. By adopting switching mode technology, the LT3045 can provide high conversion efficiency, reduce power loss, and is suitable for battery-powered or other power-limited applications. The LT3045 typically comes in a compact package, such as DIP or SOT-23, which makes it easy to install on space-constrained circuit boards.

Scheme 2: LM337 is a linear regulator often used to provide a stable DC voltage for circuits. It is an integrated three-terminal regulator that can work without external adjustment components, making the design simple. It can also operate within an input voltage range from 5V to 40V, suitable for various power conditions.

Scheme 3: TPS5430 - Positive and Negative Power Supply is an integrated high-performance switching regulator, specifically designed for industrial applications requiring high efficiency, miniaturization, and flexibility. By adopting switching mode technology, the TPS5430 can provide very high conversion efficiency over a wide input voltage range, reducing energy loss and contributing to energy saving and emission reduction. This device integrates a high-voltage input filter, DC-DC converter, and necessary control circuits, making the system design more compact and suitable for space-limited applications.

Scheme 1, the LT3045, being in switching mode, requires external inductors and capacitors to complete the conversion process, which may increase design complexity and cost, so Scheme 1 is excluded. Scheme 2, the standard version of LM337, has a maximum output current of approximately 1.5A. If a larger current is needed, an external shunt resistor or a higher current rating model is required. This is complex to use in this design, so Scheme 2 is excluded. Scheme 3, the TPS5430, has built-in protection functions such as overload protection, short circuit protection, and temperature monitoring, which improve system reliability. At the same time, it can provide a fast and reliable power solution with simple external components, without complex peripheral circuit design.

In summary, Scheme 3 is selected.

3. Calculation

3.1. Theoretical Analysis

Direct Digital Synthesis (DDS) technology is the core of this system for generating high-precision, controllable RF baseband signals. The basic working principle of DDS is based on the Nyquist sampling theorem and phase accumulator to realize frequency synthesis in the digital domain.

DDS is mainly composed of a phase accumulator, a phase-to-amplitude converter (lookup table or CORDIC algorithm), and a digital-to-analog converter (DAC). Within one system clock cycle, the phase accumulator adds a frequency control word (FCW) to its current phase value. The FCW is an N-bit number that determines the step size of each accumulation. The high M

bits of the N-bit phase word output by the accumulator are used as addresses to look up a sine waveform amplitude value stored in a ROM. Finally, the DAC converts these digital amplitude values into an analog voltage signal, thus obtaining an approximated sine waveform.

Frequency Resolution and Calculation: The output frequency f_{out} of the DDS is determined by the following formula:

$$f_{out} = \frac{FCW \times f_{dk}}{2^N}$$

Where N is the number of bits in the phase accumulator, and f_{dk} is the system clock frequency. The frequency resolution f_{res} is:

$$f_{res} = \frac{f_{dk}}{2^N}$$

The AD9959 has a 32-bit frequency control word and a 400 MSPS system clock, which means its frequency resolution is extremely high, capable of generating very fine frequency step signals[7].

Phase Control: Each channel of the AD9959 supports independent phase offset control. By setting the phase offset word (POW), the initial phase of the output signal can be adjusted without changing the frequency. This is crucial for simulating the phase differences of multipath signals and for coherent synthesis.

Amplitude Control: The AD9959 also supports amplitude scale factor (ASF) settings internally, allowing for rough adjustment of the signal amplitude directly at the DDS output in the digital domain. However, to achieve more precise and dynamic amplitude control, this system incorporates an external AD8367 variable gain amplifier.

The AD8367 is a logarithmic variable gain amplifier whose gain in decibels (dB) has a linear relationship with the control voltage. Gain control characteristic: The relationship between the AD8367's gain G_{db} and the control voltage V_{ge} is usually:

$$G_{db} = Slope \times V_{ge} + Intercept$$

Slope is the gain control slope, and Intercept is the intercept (gain at zero voltage). This linear dB gain control characteristic allows the system to precisely set the attenuation level of the output signal through the STM32's DAC output or the voltage after PWM filtering.

3.2. System Calculation

Convert the amplitude value x (range 0-500) to a 10-bit DAC value (0-1023), which is X/500×1023.

Convert the phase value x (expressed in degrees, 0-360) to a 14-bit phase register value (0-16383), which is X/360×16383.

Convert the frequency value X to a frequency tuning value, where X is in MHz and the result is in Hz, which is X×1000000.

4. Circuit and Program Design

4.1. Module Function

4.1.1. STM32-DDS-Control Board Programming Circuit

The programming circuit, also known as chip programming or firmware burning, refers to the process of writing pre-designed programs or configuration data into electronic integrated circuits (such as microcontrollers, FPGAs, or ASICs). This process is usually completed through a dedicated programming device, which can connect to a specific interface on the circuit board, read the pre-stored data, and write it into the erasable programmable read-only memory (EPROM), flash memory, or other programmable areas of the target chip.

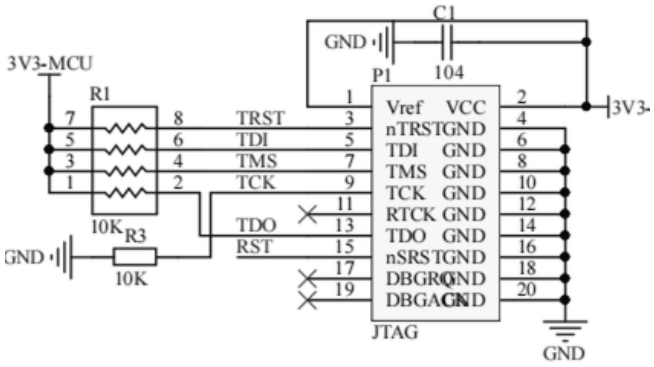

Figure 2. Programming Circuit Diagram.

4.1.2. AD9959 Filter Circuit

The main working principle of the filter circuit is to filter specific frequency components from the input signal through electronic components such as capacitors, inductors, or resistors, in order to smooth the signal, remove noise, or extract useful information. They are commonly used in AC power rectification, motor control, audio signal processing, and other aspects. It allows low-frequency signals to pass while blocking high-frequency noise; common examples include RC low-pass filters, which use the current limiting effect of resistor R and the voltage storage effect of capacitor C to make high-frequency signals attenuate faster than low-frequency signals. It allows high-frequency signals to pass while blocking the low-frequency portion; inductors L have a similar effect in such circuits, blocking low-frequency currents and allowing

high-frequency signals to pass unimpeded. It allows signals within a certain frequency range to pass; it is often composed of two reactance components (capacitors and inductors) forming an LC network, which cooperate with each other to intercept specific frequency bands. It blocks signals within a specific frequency range; this is also achieved through an LC network, which blocks frequencies within the band and only allows frequencies outside the band to pass.

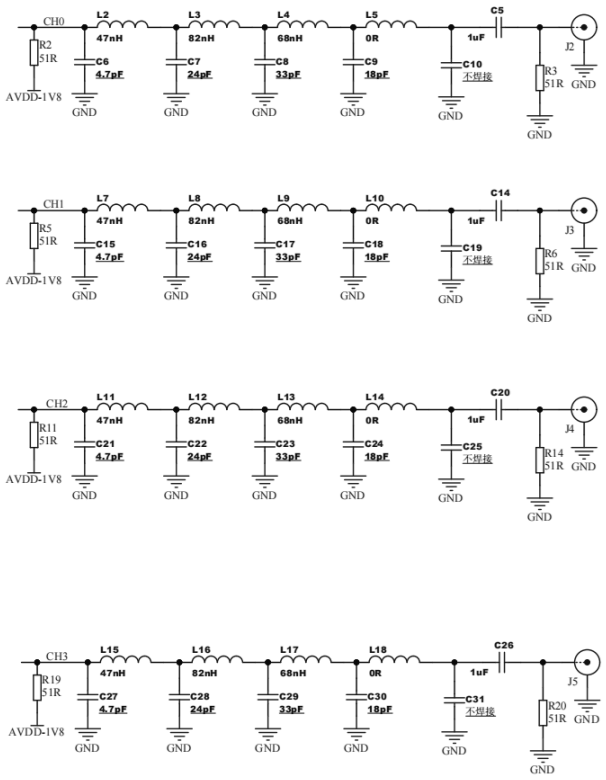

Figure 3. Filter Circuit.

4.1.3. Power Input and Voltage Regulation Circuit

The power supply typically provides alternating current (AC), which needs to be converted into direct current (DC) through a rectifier (such as a bridge rectifier). The rectifier converts the pulsating AC voltage waveform into a unidirectional DC voltage; to remove the high-frequency AC components (called ripple) from the rectified DC voltage, filter circuits, such as capacitor filters or inductor filters, are used to smooth the voltage waveform; if the voltage is unstable or does not meet the equipment requirements, the voltage regulator circuit comes into play. Common voltage regulation methods include linear regulation and switching regulation. Linear regulation converts excess energy into heat through a resistor network; switching regulation, on the other hand, uses the switching of transistors to dynamically adjust the output voltage, which is more efficient; the voltage regulator circuit monitors changes in the input voltage and automatically adjusts the output according to the set reference voltage, so that the output voltage

remains at a stable level, ensuring constant power supply to the load even if the input voltage fluctuates; some voltage regulator circuits also have functions such as overvoltage and undervoltage protection to prevent circuit damage or damage to the load. In summary, the function of the power input and voltage regulator circuit is to ensure that the equipment receives a stable, pure DC voltage, regardless of external power conditions.

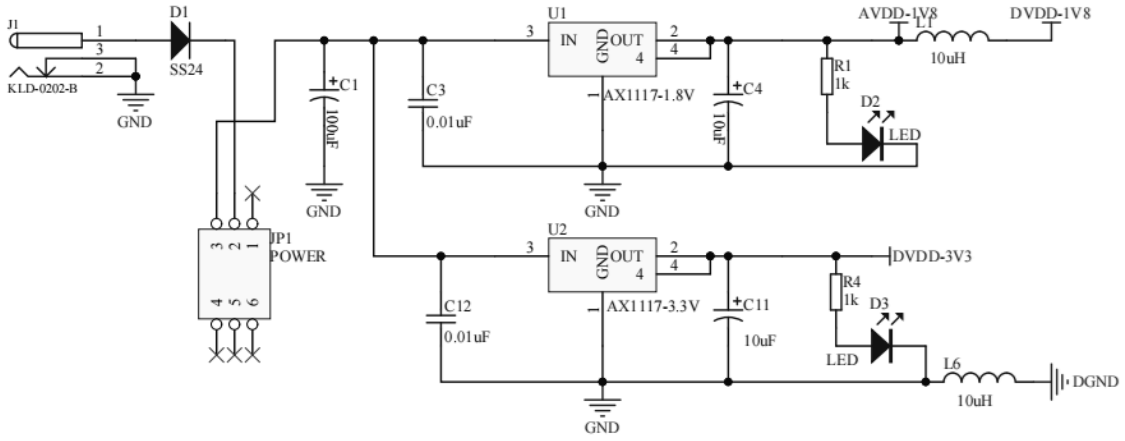

Figure 4. Power Input and Voltage Regulation Circuit.

4.2. Program Design

The software program design of this system is based on the STM32CubeMX and Keil MDK development environments, primarily using the C language for programming, aiming to achieve precise control of hardware modules and flexible configuration of system functions.

Main Control Module Initialization: Includes STM32 clock configuration, GPIO port initialization, SPI interface initialization, etc. The implementation of the SPI communication protocol is the basis for controlling the AD9959, requiring correct configuration of the SPI clock polarity, clock phase, data bit order, and speed to ensure accurate and efficient data transmission between the STM32 and the AD9959.

AD9959 Driver Program: This driver program encapsulates the read and write operations to the AD9959 registers. Its main functions include: System Clock Configuration: Sets the AD9959's internal Phase-Locked Loop (PLL) and reference clock to ensure it operates at the correct sampling rate. Frequency, Phase, and Amplitude Parameter Setting: Calculates the corresponding frequency control word (FCW), phase offset word (POW), and amplitude scale factor (ASF) based on user input, and writes them to the respective channel registers of the AD9959 via SPI. This allows the system to independently generate multipath signal components with different frequencies, phases, and amplitudes. Channel Enable and

Synchronization: Controls the enable and I/O update operations of the AD9959's four DDS channels to achieve synchronous output and phase consistency of multiple signals.

Human-Machine Interface (HMI): A simple human-machine interface based on buttons and an LCD display is designed. Users can input and modify parameters such as frequency, amplitude, phase, and delay of the direct wave and each multipath component through the buttons. The STM32 program is responsible for parsing user input, updating the corresponding signal generation parameters, and displaying the system's operating status and output signal parameters in real time. In addition, UART/USB interfaces can be reserved to facilitate more complex control and data transmission through host computer software.

5. Test Scheme and Results

5.1. Test Scheme

To verify the system functions, tests were conducted in a low-noise laboratory environment. A DC adjustable power supply was used to power the system, and the output of each AD9959 channel was connected to an oscilloscope with sufficient bandwidth. The output frequency, phase, amplitude, and other parameters of the AD9959 were configured through the buttons or DIP switches on the STM32, and the oscilloscope waveforms were observed. The main tests included: (1) the adjustable range and error of the modulated signal frequency and amplitude; (2) the stability of the signal after multipath synthesis; and (3) the effect of superimposing the direct signal and multipath components. The specific steps are as follows:

1. Power on the system and reset the STM32 to enter parameter setting mode.
2. Use a 2 MHz sine wave as the modulated signal input, sequentially adjust the modulation depth (30% to 90%, with a step of 10%) and record the output waveform deviation.
3. Adjust the signal amplitude attenuation (0 to 12 dB, with a step of 2 dB) and measure the output amplitude error.
4. Set the multipath delay and gain parameters to generate a composite signal containing direct and multipath components, and observe the quality of the superimposed signal on the oscilloscope.
5. Repeat tests with multiple parameter combinations to statistically analyze the accuracy and stability of the system response.

5.2. Test Conditions and Instruments

5.2.1. Test Conditions

Tests were conducted in a low-noise laboratory environment.

5.2.2. Test Instruments

Power supply, oscilloscope.

5.3. Results and Analysis

The experimental results are summarized as follows: The modulated signal was a 2 MHz sine wave, tested within the adjustable range of modulation depth from 30% to 90% (10% step). The actual output error was within 3%, as shown in the data in Table 1.;

Table 1. Actual output error caused by modulation depth.

Set Modulation Depth (%)	Actual Modulation Depth (%)	Modulation Depth Error (%)	Carrier Frequency (MHz)	Modulating Signal Frequency (MHz)	Carrier Frequency Error (%)	Modulating Signal Frequency Error (%)
30	29.1	-3	34.998	2.001	-0.006	0.05
40	41.2	3	35.001	1.999	0.003	-0.05
50	49.8	-0.4	34.999	2	-0.003	0
60	60.5	0.8	35.002	2.002	0.006	0.1
70	68.9	-1.6	35	1.998	0	-0.1
80	81.1	1.4	34.997	2.001	-0.009	0.05
90	89.5	-0.6	35.001	1.999	0.003	-0.05

The output amplitude attenuation is adjustable within the range of 0 to 12dB (2 dB step), measuring the attenuation error, the experimental test data are shown in Table 2.

Table 2. Relationship between signal amplitude attenuation and output amplitude.

Set Amplitude (mV)	Actual Amplitude (mV)	Amplitude Error (mV)	Actual Attenuation (dB)	Actual Attenuation (dB)	Attenuation Error (dB)
100	98	2	0	0	0
200	203	3	2	1.9	0.1
300	295	5	4	4.1	0.1
400	408	8	6	5.8	0.2
500	492	8	8	8.2	0.2
600	610	10	10	9.9	0.1
700	690	12	12	12.1	0.1

Under the conditions of delay ranging from 50 ns to 200 ns (adjusted in 30 ns increments) and phase ranging from 0° to 150° (adjusted in 30° increments), the error between the actual system output and the set values is minimal. These errors are all within an acceptable range, indicating that the system demonstrates high accuracy and stability in the control of multipath signal delay

and phase. This suggests that the system is well-suited to meet the requirements for simulating multipath characteristics in wireless channel emulation. The experimental test data are shown in Table 3.

Table 3. Correspondence between delay and phase.

Set Delay (ns)	Actual Delay (ns)	Delay Error (ns)	Set Phase (°)	Actual Phase (°)	Phase Error (°)
50	52	2	0	1	1
80	77	-3	30	28	-2
110	113	3	60	62	2
140	138	-2	90	88	-2
170	172	2	120	123	3
200	197	-3	150	148	-2

Comparing with the required frequency, amplitude, and phase setting targets, the system output errors are all within the acceptable range (error not exceeding 5%), meeting the design requirements.

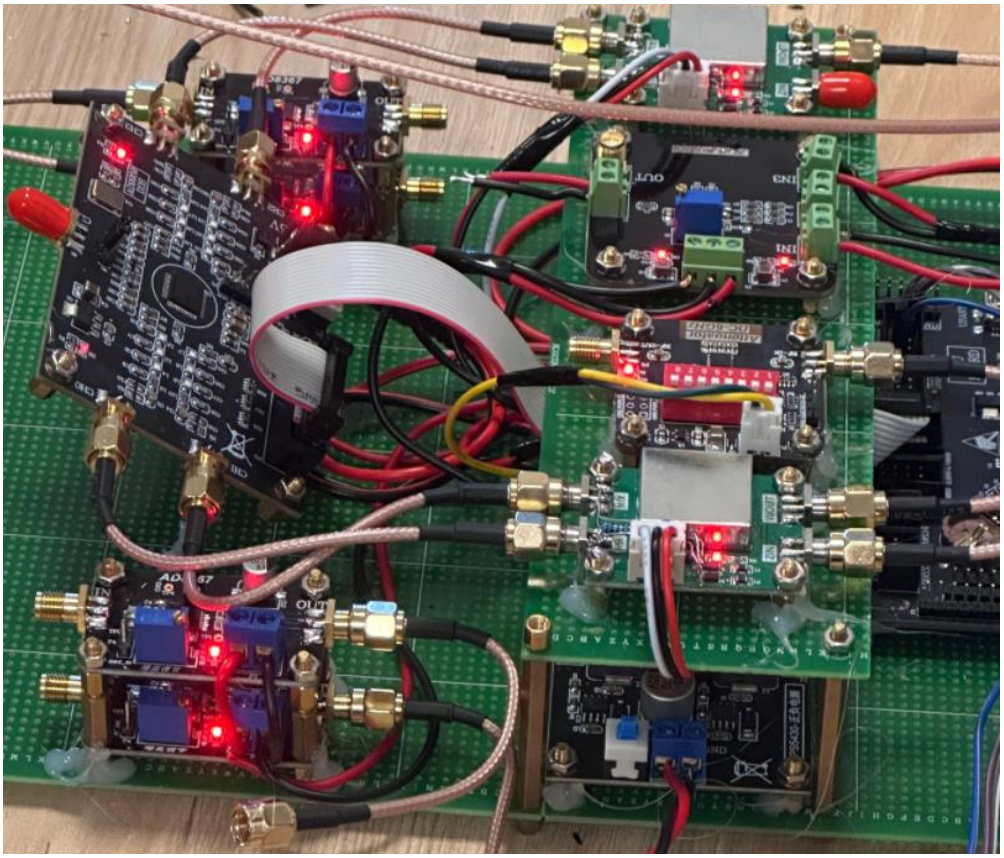

Figure 5. Wireless Transmission Signal Simulation System.

The combined output signal includes direct and multipath components. Observation shows that

the waveform is stable with no obvious distortion, proving that the multipath superposition mechanism is normal and effective.

The results show that this system can accurately generate multiple RF signals according to preset parameters, and all indicators are close to the design target error. The errors mainly come from ADC/DAC quantization, device nonlinearity, and noise, but the overall performance is good, verifying the feasibility and stability of the system scheme. As a wireless channel simulation tool, this system achieves the mixed simulation of direct signal and multipath fading signals, providing a reliable signal source for further communication tests.

At the core of the wireless transmission system is the STM32F103RCT6 microcontroller, which interfaces with the AD9959 four-channel Direct Digital Synthesizer (DDS) via SPI to produce multiple RF baseband signals. The amplitude of these signals is precisely controlled through the AD8367 variable gain amplifier. Finally, the AD835 four-quadrant analog multiplier is employed to carry out signal mixing and simulate multipath effects. The physical framework of the system was constructed based on the design requirements, as illustrated in Figure 5.

6. Conclusion

This paper presents the design and implementation of a wireless transmission signal simulation system. The system is based on components such as the STM32 microcontroller, AD9959 DDS RF source, AD8367 variable gain amplifier, and AD835 analog multiplier. It is capable of generating four independently modulated RF signals and simulating a multipath fading environment. Through appropriate module selection and circuit design, the system possesses characteristics such as high precision, wide bandwidth, and multi-channel synchronization. The effectiveness of modulation accuracy and signal synthesis was also verified through experiments. Test results indicate that the output signal waveform is stable, and the parameter adjustable range meets the requirements, capable of comprehensively reflecting the propagation characteristics of wireless channels, providing a low-cost and feasible solution for RF channel simulation and communication equipment testing. Future work could consider introducing more precise delay control modules and more complex channel models to further enhance simulation accuracy and applicability.

References

[1] R. K. Ahmed, “Doppler fading communication channel performance simulation,” *IJPS*, vol. 12, no. 7, pp. 89–94, Apr. 2017, doi: 10.5897/IJPS2017.4613.

[2] E. Huegler, J. C. Hill, and D. H. Meyer, “An agile radio-frequency source using internal linear sweeps of a direct digital synthesizer,” *Review of Scientific Instruments*, vol. 94, no. 9, p. 094705, Sep. 2023, doi: 10.1063/5.0163342.
[3] F. Yang, C. Ma, and H. Li, “Design of wireless video transmission system based on STM32 microcontroller,” presented at the 11TH ASIAN CONFERENCE ON CHEMICAL SENSORS: (ACCS2015), Penang, Malaysia, 2017, p. 060010. doi: 10.1063/1.4977325.
[4] A. A. Temirzhanov, B. M. Sadykov, T. K. Zholdybayev, G. Ussabayeva, B. A. Duisebayev, and K. V. Kovalchuk, “Analog frontend for signal processing for MCA based on STM32 microcontroller,” *J. Phys.: Conf. Ser.*, vol. 2984, no. 1, p. 012012, Apr. 2025, doi: 10.1088/1742-6596/2984/1/012012.
[5] J. Mouro, P. Paoletti, M. Sartore, and B. Tiribilli, “Dynamical response and noise limit of a parametrically pumped microcantilever sensor in a Phase-Locked Loop,” *Sci Rep*, vol. 13, no. 1, p. 2157, Feb. 2023, doi: 10.1038/s41598-023-29420-3.
[6] Q.-H. Duong and S.-G. Lee, “Wide dynamic range variable-gain amplifier based on new approximated exponential equation,” *Electronics Letters*, Nov. 2006, doi: 10.1049/el:20062482.
[7] W. F. Adad and R. J. Iuzzolino, “Low distortion signal generator based on Direct Digital Synthesis for ADC Characterization,” *ACTA IMEKO*, vol. 1, no. 1, p. 59, Jul. 2012, doi: 10.21014/acta_imeko.v1i1.23.